AMENDMENTS TO THE CLAIMS

1. (original) An arrangement of differential pairs for eliminating crosstalk in a printed circuit board having a plurality of layers, comprising:

a dielectric material;

a first differential pair disposed in said dielectric material, further comprising a first signal trace and a second signal trace; and

a second differential pair disposed in said dielectric material, further comprising a third signal trace and a fourth signal trace; wherein

said first signal trace is disposed in one of the plurality of layers, while said second signal trace is disposed in another one of the plurality of layers; and

wherein said fourth signal trace is disposed in one of the plurality of layers where said first signal trace is disposed therein, while said third signal trace is disposed in another one of the plurality of layers where said second signal trace is disposed therein.

2. (withdrawn) The arrangement as recited in claim 1, wherein said second differential pair is disposed in one of the plurality of layers different from that of said first signal trace and said second signal trace.

3. (withdrawn) The arrangement as recited in claim 2, wherein said first differential pair and said second differential pair form a diamond shape.

4. (canceled)

5. (currently amended) The arrangement as recited in claim [[4]] 1, wherein said first differential pair and said second differential pair form a rectangular shape.

6. (withdrawn) An arrangement of differential pairs for eliminating crosstalk in a printed circuit board having a plurality of layers, comprising:

a dielectric material;

a first differential pair, further comprising a first signal trace and a second trace;

and

a second differential pair, further comprising a third signal trace and a fourth signal trace; wherein

at least one of said first signal trace, said second signal trace, said third signal trace and said fourth signal trace is disposed on said dielectric material, while each of the remaining of said first signal trace, said second signal trace, said third signal trace and said fourth signal trace is disposed in one of the plurality of layers.

7. (withdrawn) The arrangement as recited in claim 6, wherein said first signal trace and said fourth signal trace are disposed on said dielectric material, while said second signal trace and said third signal trace are disposed in said dielectric material, the third signal trace being substantially below the first signal trace and the second signal trace being substantially below the fourth signal trace.

8. (withdrawn) The arrangement as recited in claim 6, wherein said first signal trace is disposed on the dielectric material, while said second signal trace is disposed in one of the plurality of layers and said second differential pair is disposed in one of the plurality of layers.

9. (withdrawn) The arrangement as recited in claim 6, wherein said first signal trace and said second differential pair are disposed on the dielectric material, while said second signal trace is disposed in one of the plurality of layers.

10. (withdrawn) An arrangement of differential pairs for eliminating crosstalk in a printed circuit board having a plurality of layers, comprising:

a dielectric material;

a first differential pair disposed in said dielectric material, further comprising a first signal trace and a second trace;

a second differential pair; and

a first ground plane disposed in said dielectric material; wherein said second differential pair is substantially above said first ground plane.

11. (withdrawn) The arrangement as recited in claim 10, wherein said second differential pair is disposed in said dielectric material, while the first differential pair is substantially below said first ground plane.

12. (withdrawn) The arrangement as recited in claim 10, further comprising a second ground plane, wherein said second ground plane and said second differential pair are disposed on said dielectric material, said first differential pair being substantially below said second ground plane and said second differential pair being substantially above said first ground plane.

13. (withdrawn) The arrangement as recited in claim 10, further comprising a second ground plane and a third ground plane, wherein said second ground plane, said third ground plane and said second differential pair are disposed on said dielectric material, while said first ground plane is disposed between said first signal trace and said second trace, said first signal trace being substantially below said second ground plane, said second signal trace being substantially below said third ground plane, and said second differential pair being substantially above said first ground plane.

14. (original) A printed circuit board comprising:

a substrate defining different levels along a vertical direction thereof, said substrate integrally equipped with first and second differential pairs closely arranged with each other,

said first different pair defining spaced first and second traces,

said second differential pair defining spaced third and fourth traces,

the first trace and the second trace being located at different first and second levels; wherein

an intersection angle between a first line linking center points of the first trace and

the second trace, and a second line linking center points of the third trace and the fourth trace, is neither zero nor ninety.

15. (currently amended) The printed circuit board as recited in claim 14, wherein the fourth trace is located at the same first level with the ~~second~~ first trace, and the third trace is located at ~~the~~ a same second level with the ~~first~~ second trace.

16. (withdrawn) The printed circuit board as recited in claim 14, wherein the first level is essentially located on the substrate and exposed to an exterior while the second level is embedded in the substrate.

17. (withdrawn) The printed circuit board as recited in claim 14, wherein a width of the first trace is different from that of the second trace.

18. (original) The printed circuit board as recited in claim 14, wherein a cross-sectional configuration of the traces is rectangular having a long side in a horizontal direction and a short side in the vertical direction.

19. (original) The printed circuit board as recited in claim 18, wherein a distance between the two center points of the first differential pair in the vertical direction is smaller than that in the horizontal direction.

20. (withdrawn) A printed circuit board comprising:

a substrate defining different levels along a vertical direction thereof, said substrate integrally equipped with first and second differential pairs closely arranged with each other,

said first different pair defining spaced first and second traces,

said second differential pair defining spaced third and fourth traces,

the first trace and the second trace being located at different first and second levels;

an intersection angle between a first line linking center points of the first trace and the second trace, and a second line linking center points of the third trace and the fourth trace, being ninety; wherein

said first level is essentially on the substrate while said second level is essentially in the substrate, and a width of the first trace which is exposed to an exterior is different from that of the second trace which is embedded in the substrate.

21. (withdrawn) The printed circuit board as recited in claim 20, wherein the third trace and the fourth trace are at a same level which is either the first level or the second level.

22. (withdrawn) The printed circuit board as recited in claim 21, wherein the widths of said third trace and said fourth traces are essentially equal to either that of the first trace if said third and fourth traces are at the first level, or that of the second trace if said third and fourth traces are at the second level.

23. (withdrawn) A printed circuit board comprising:

a substrate defining different levels along a vertical direction thereof, said substrate integrally equipped with first and second differential pairs closely arranged with each other,

said first different pair defining spaced first and second traces,

said second differential pair defining spaced third and fourth traces,

the first trace and the second trace being located at a same first level, and the third and fourth traces being located at a same second level;

an intersection angle between a first line linking center points of the first trace and the second trace, and a second line linking center points of the third trace and the fourth trace, being zero;

wherein the first differential pair are not aligned with the second differential pair in the vertical direction but in an offset manner so that the second trace results in a negligible crosstalk to the fourth trace which is more distant from the second trace than the third trace.

24. (withdrawn) The printed circuit board as recited in claim 23, wherein a grounding plane is provided beside the first differential pair at the same first level and in alignment with the second differential pair in said vertical direction

so as to absorb the crosstalk resulting from the second trace and the third trace.

25. (withdrawn) The printed circuit board as recited in claim 24, wherein another grounding plane is provided beside the second differential pair at the same second level and in alignment with the first differential pair in said vertical direction for absorb the crosstalk resulting from the second trace and the third trace.

26. (withdrawn) The printed circuit board as recited in claim 23, wherein the third trace and the fourth trace are far away spaced from each other with therebetween a space which is aligned with the first differential pair.

27. (withdrawn) The printed circuit board as recited in claim 26, wherein a grounding plane is provided either in said space at said second level, or by one side of said first differential pair at the first level and in alignment with one of said third and fourth traces in the vertical direction.

28. (withdrawn) The printed circuit board as recited in claim 23, wherein said first level is essentially on the substrate while said second level is essentially in the substrate, and a width of the first trace which is exposed to an exterior is different from that of the third trace which is embedded in the substrate.